Homework 2

(Due date: October 4th)

Presentation and clarity are very important! Show your procedure!

PROBLEM 1 (36 PTS)

- Calculate the result (provide the 32-bit result) of the following operations with 32-bit floating point numbers. Truncate the results when required. When doing fixed-point division, use 8 fractional bits. Show your procedure.

✓ 40C00000 + C2EA9000	✓ 5A09D378 – 4C490FD8	✓ 7A09D300 × 4D080000	✓ 800C0000 ÷ 494C0000
✓ 10DAD000 + 10FAD000	✓ 801BEEDA – 7F800000	✓ 90DECADE × FF800000	✓ 7F800000 ÷ 800ABBAA
✓ 801A8000 + 92CE8000	✓ BA09D380 – 39DEC0DE	✓ 0B09A000 × 8FACC000	✓ C9746000 ÷ 40490000

PROBLEM 2 (8 PTS)

- Complete the table for the following DFX formats:

DFX format	p_0	p_1	Number of bits of significand	Boundary value	$num0$ range	$num1$ range	Dynamic Range (dB)
8_3_2							
16_12_4							
24_16_8							
32_24_16							

PROBLEM 3 (16 PTS)

- Convert the following signed fixed point numbers in format [16 8] to the dual fixed point format 16_8_3. If more bits are required, you are allowed to use the format 17_8_3.

FX	FA.CE	04.2F	8D.EE	AF.27	81.BE	80.E4	8A.BB	AB.CE
DFX								

PROBLEM 4 (30 PTS)

- Calculate the result of the following operations where the numbers are represented in dual fixed-point arithmetic. Note that the results must be in the same format. Include an overflow bit when necessary.

DFX Format: 8_4_2	Result	overflow		Result	overflow
FA+09			EB+AF		
E2+BB			C0-C2		
FB-7A			F8+3A		

DFX Format 16_8_4	Result	overflow		Result	overflow
FA2A+0A09			F939-0932		
C000+F1C3			F343-6AA9		
F990-0A32			D001+F170		

PROBLEM 5 (10 PTS)

- Complete the timing diagram of the following iterative unsigned multiplier ($N = 4, M = 4$).
  Register: $sclr$: synchronous clear. Here, if $sclr = E = 1$, the register contents are initialized to 0.
  Parallel access shift register: If $E = 1$: $s\_l = 1 \rightarrow$ Load, $s\_l = 0 \rightarrow$ Shift